

Remarks

Applicants respectfully request that this amendment be entered, and that their subject U.S. Patent application be passed to issuance in view thereof. The foregoing amendments are further indicated in blackline form in Exhibit A, VERSION WITH MARKINGS TO SHOW CHANGES MADE.

In the Office Action, claims 23-27 stand rejected under 35 U.S.C. 102(b) as being anticipated by Juang et al (TW 2898436). For the reasons set forth below, Applicants respectfully submit that this reference neither teaches nor suggests the invention.

With reference to claim 23, note that the invention is recited as including diffusion regions that are adjacent the extension regions so as to expose a portion of one of the extension regions at a surface of the semiconductor layer. Applicants respectfully submit that no such construct is shown in the Juang reference. In the Office Action the Examiner suggests that n-doped diffusions 15 are the extension regions. That would mean that some other diffusion regions would have to serve as the recited "diffusion regions that are adjacent the extension regions so as to expose a portion of one of the extension regions at a surface of the semiconductor layer." First, consider the diffusion 16 disposed in a portion of the substrate to the right of the gate. Diffusion region 16 is n+ doped, meaning that as a practical matter it will replace any portion of n-doped region 15 in any place where the two are co-extensive. Since region 16 is shown as extending further beneath the gate than the applicable region 15, as a practical matter after region 16 is formed there will be no region 15 in that area (and hence, no portion of region 15 is "exposed" by region 16, as recited). Now consider dopant region 19, disposed in a portion of the substrate to the left of the gate. Note that the remaining portion of region 15 to the left of the gate is not exposed at a surface of the semiconductor layer is protected by the sidewall spacer disposed above it, such that NO portion of region 15 to the left of the gate is exposed at the substrate surface. Thus, neither diffusion region 16, nor diffusion region 19, illustrate the recited diffusion region since the Juang

reference does not illustrate all of the recited features of the invention as recited in claim 23, Applicants respectfully submit that the rejections of record to their claim 23 (as well as to dependent claims 24-27) based on Juang have been traversed.

In the Office Action, claims 23-25 and 27 stand rejected under 35 U.S.C. 102(e) as being anticipated by the Hsu reference (USP 6,211,001). For the reasons set forth below, Applicants respectfully submit that this reference neither teaches nor suggests the invention. Claim 23 recites that the structures of the invention are formed on a semiconductor layer disposed on an insulator layer. Such a construct is not shown in Hsu; the substrate appears to be of the conventional bulk, single crystal silicon type (see e.g. Col. 3, lines 29-30: "Device 60 is formed on a substrate of single crystal silicon 66."). As such, Applicants respectfully submit that the Hsu structure is not applicable to the present invention, because it is only in the recited SOI context that the body charges build up (as opposed to being dissipated, as in substrates such as that shown in Hsu). See pages 1-2 of the present specification. Accordingly, Applicants respectfully submit that the rejections of record to claim 23 (as well as claims 24, 25, and 27 dependent thereon) under 35 USC 102(e) based on Hsu have been traversed.

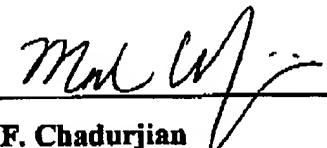
Applicants have submitted new claims 28-33. Applicants respectfully submit that these claims do not represent new matter, because all of these claims are supported by the specification and claims as originally filed. Dependent claims 28-31 depend directly or indirectly on claim 23; as such, the foregoing arguments as to the patentability of claim 23 apply to these claims as well. In new independent claim 32, Applicants have recited a combination of features that is neither taught nor suggested by any of the prior art of record; accordingly, Applicants respectfully submit that claim 32, along with its dependent claim 33, recites allowable subject matter.

In view of the foregoing, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments, questions, or suggestions, please do not hesitate to contact the undersigned attorney at the telephone number and/or email address set forth below.

**Respectfully submitted,**

**For:** Bryant et al.

**By:**

  
**Mark F. Chadurjian**

**Reg. No. 30,739**

**Telephone: (802) 769-8843**

**Facsimile (802) 769-8938**

**Email: mchadurj@us.ibm.com**

**IBM Corporation, IPLaw Dept. 972E  
1000 River Street  
Essex Junction, VT 05452**

**FAX RECEIVED**

**JAN 13 2003**

**TECHNOLOGY CENTER 2800**

**BUR919990055US2**

**5**

**S/N 09/978,528**

Exhibit AVERSION WITH MARKINGS TO SHOW CHANGES MADEIn the Claims:

Kindly add the following new claims 28-33, as follows:

28. (New) The device according to claim 23, wherein said extension regions extend further under the spacers than said diffusion regions.
29. (New) The device according to claim 23, wherein said metal layer and said exposed portion of the extension region form a Schottky diode.
30. (New) The device according to claim 29, wherein said metal layer extends into the semiconductor layer.
31. (New) The device according to claim 30, wherein said metal layer extends into a portion of the semiconductor layer below said extension regions.
32. (New) An integrated circuit disposed on an SOI substrate having a body region, comprising a transistor having a source diffusion region, a gate formed over said body region, a first sidewall spacer disposed on a sidewall of said gate abutting said source diffusion region, a drain diffusion region, a second sidewall spacer disposed on a sidewall of said gate abutting said drain diffusion region, wherein said first sidewall spacer is thinner than said second sidewall spacer, and extension diffusion regions that extend further under said gate than said source diffusion region or said drain diffusion region, said extension diffusion regions having a dopant concentration less than that of said source diffusion region and said drain diffusion region; and a conductor in contact with at least a portion of at least one of said extension regions and at least a portion of said source diffusion region to form a Schottky diode that prevents charge from accumulating in said body region.
33. (New) The device of claim 32 wherein said conductor is in contact with said body region.

BUR919990055US2

6

S/N 09/978,528